



IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Re the Application of:

MOHAMMAD ABDALLAH, ET AL.

Application No.: 09/852,217

Filed: May 8, 2001

For: **Executing Partial-Width Packed Data
Instructions**

Art Group: 2183

Examiner: Coleman, Eric

INFORMATION DISCLOSURE STATEMENT UNDER 37 C.F.R. §1.97

Commissioner for Patents
P.O. Box 1450
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In accordance with the duty of disclosure, enclosed is a copy of IDS Citation Form PTO/SB/08 or PTO-1449, together with copies of the documents cited on that form, except for copies not required to be submitted (e.g., copies of U.S. patents and U.S. published patent applications need not be enclosed). This IDS and IDS Citation Form are being submitted concurrently with the Reexamination Continuation Application. It is respectfully requested that the cited references be considered and that the enclosed copy of PTO/SB/08 be initialed by the Examiner to indicate such consideration and a copy thereof returned to applicant(s).

The submission of this Information Disclosure Statement is not to be construed as a representation that a search has been made in the subject application and is not to be construed as an admission that the information cited in this statement is material to patentability.

Please charge any fees due to Deposit Account 02-2666. A duplicate copy of the Fee Transmittal (PTO/SB/17) is enclosed for this purpose.

Respectfully submitted,

BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN LLP

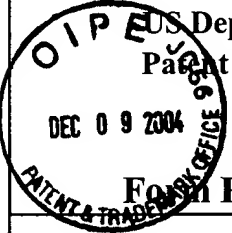
Date: 12-6-04

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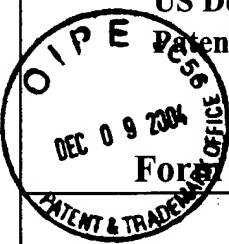
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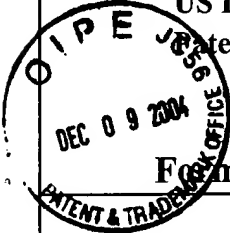
Krista Mathieson Dec. 6, 2004
Krista Mathieson *Date*

				Atty. Docket No.: 42390.P5193C		Application No.: 09/852,217	
				Applicant: Abdallah et al.			
				Filing Date: May 8, 2001			
US Patent Documents							
Examiner's Initials		Date	Document Number	Name	Class	Sub- Class	Filing Date
		07/31/90	4,945,479	Rusterholz et al.			
		11/20/90	4,972,362	Elkind et al.			
		09/10/91	5,047,975	Patti et al.			
		01/14/92	5,081,698	Kohn			
		11/30/92	5,161,247	Murakami et al.			
		02/23/93	5,189,636	Patti et al.			
		07/05/94	5,327,369	Ashkenazi			
		02/14/95	5,390,135	Lee et al.			
		05/07/96	5,515,520	Hatta et al.			
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		04/20/04	6,725,356	Hansen et al.			
Foreign Patent Documents							
Examiner's Initials		Date	Document Number	Country	Class	Sub- Class	Translation
Other Documents (Including Author, Title, Date, Pertinent Pages, etc.)							
<i>Examiner</i>				<i>Date Considered</i>			

Examiner: Initial if reference is considered, whether or not citation is in conformance with MPEP 609; Draw a line through the citation if not in conformance and not considered. Include a copy of this form with the next communication to the applicant

 <p style="margin: 0;">US Department of Commerce Patent and Trademark Office Form PTO-1449 (Modified)</p>			Atty. Docket No.: 042390.P5193C		Application No.: 09/852,217		
			Applicant: Abdallah et al.				
			Filing Date: May 8, 2001				
US Patent Documents							
Examiner's Initials		Date	Document Number	Name	Class	Sub- Class	Filing Date
Foreign Patent Documents							
Examiner's Initials		Date	Document Number	Country	Class	Sub- Class	Translation
Other Documents (Including Author, Title, Date, Pertinent Pages, etc.)							
		Santoro, Mark; Design and Clocking of VLSI Multipliers. Technical Report No. CSL -TR-89-397, October 1989. Pages i-xii and 1-118.					
		Santoro, Mark, et al.; SPIM: A Pipelined 64X64 bit Interactive Multiplier, IEEE Journal of Solid -State Circuits, Vol. 24, No. 2, April 1989. Pages 487-493.					
		Santoro, Mark, et al.; SESSION II: HIGH-SPEED MICROPROCESSOR. WAM 2.6: A Pipe-lined 64X64b Interactive Array Multiplier. 1988 IEEE International Solid State Circuits Conference . Pages 36-37 and 290.					
		BIT Preliminary, Bipolar Integrated Technology, Inc. B3110/B3120;B2110/B2120 Floating Point Chip Set. Pages 1-40.					
		Eklind, Bob, et al. A SUB 10 nS Bipolar 64 Bit Integrated/Floating Point Processor Implemented On Two Circuits. IEEE 1987 BCTM, pages 101- 104					
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		Farmwald, P. Michael; High Bandwidth Evaluation of Elementary Functions, S-1 Project. IEEE 1981. Pages 139 - 142.					
		Farmwald, P. Michael; On the Design of High Performance Digital Arithmetic Units. UCRL-53190. August 1981. Pages i-vii and 1-95.					
		Grimes et al.; 64-Bit Processor. The Intel i860 64-Bit Processor: A General-Purpose CPU with 3D Graphics Capabilities. July 1989. Pages 85-94.					
Examiner			Date Considered				

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			042390.P5193C		09/852,217		
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Examiner's Initials		Date	Document Number	Country	Class	Sub- Class	Translation
Other Documents (Including Author, Title, Date, Pertinent Pages, etc.)							
		Ide, et al.; A 320-MFLOPS CMOS Floating-Point Processing Unit for Superscalar Processors. IEEE Journal of Solid State Circuits, Vol. 28, No. 3, March 1993. Pages 352 - 361.					
		Lino, et al.; ISSCC 92 SESSION 6/ MICROPROCESSORS/ TA 6.5: A 289MFLOPS Single-Chip Supercomputer. 1992 IEEE International Solid State Circuits Conference. Pages 112-113.					
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		Lee, Ruby B.; Realtime MPEG Video via Software Decompression on a PA-RISC Processor. 1995 IEEE, pages 186-192.					
		Manferdelli, John L. et al.; Signal Processing Aspects of the S-1 Multiprocessor Project. UCRL-84658. July 28, 1980. Pages 1-8.					
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		Undy, Steve, et al.; A Low-Cost Graphics and Multimedia Workstation Chip Set. April 1994, IEEE micro, pages 10 - 22.					
Examiner				Date Considered			

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